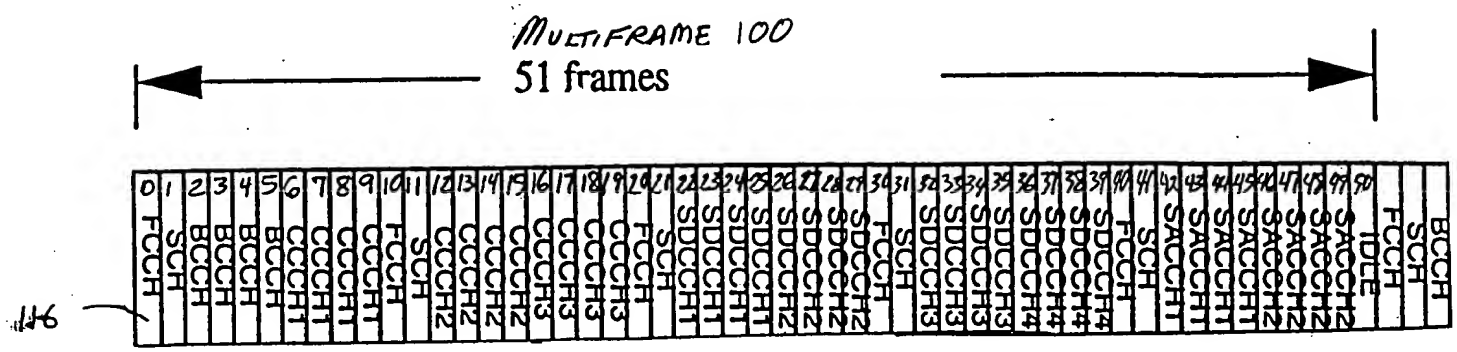


FIGURE 1

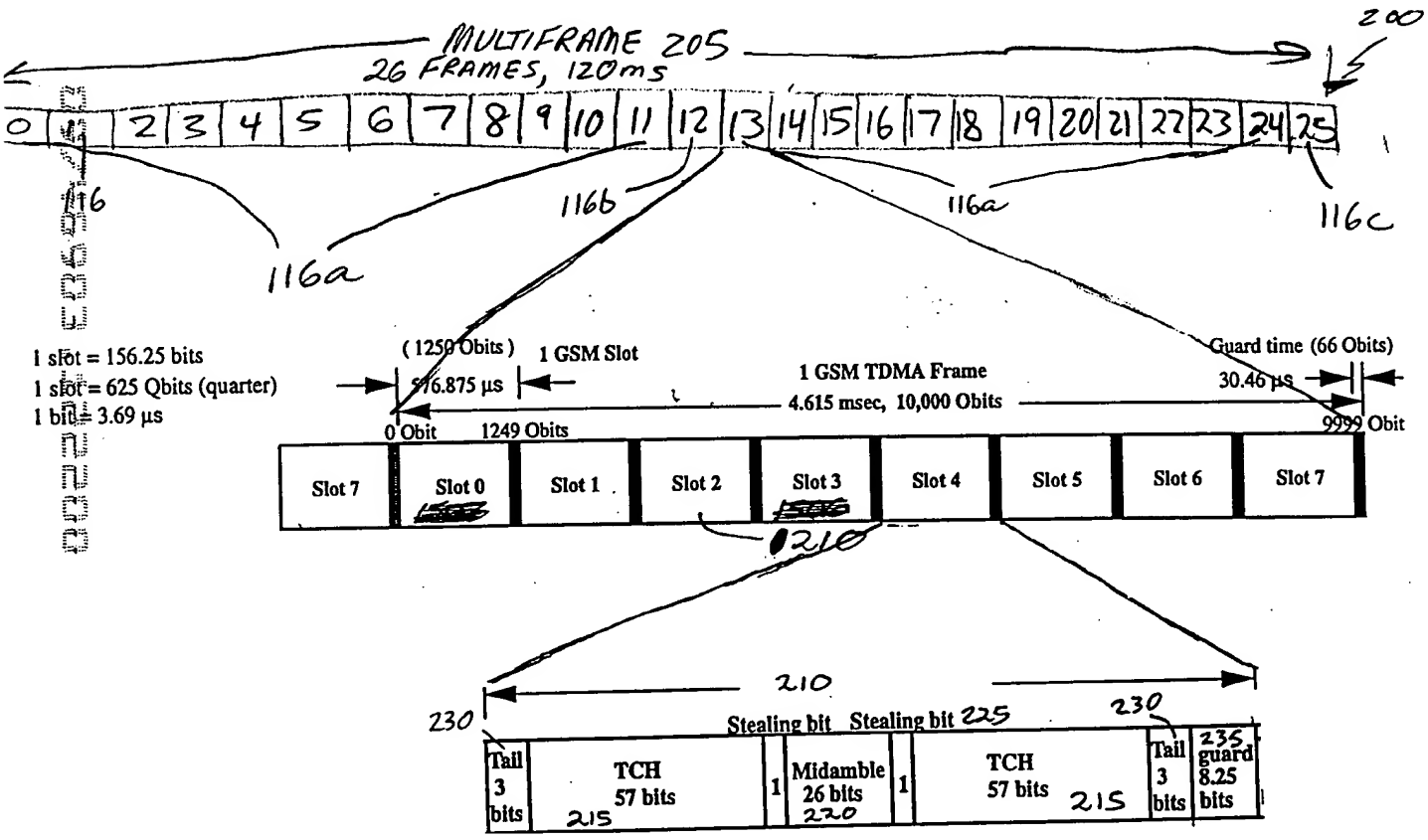


FIGURE 2A

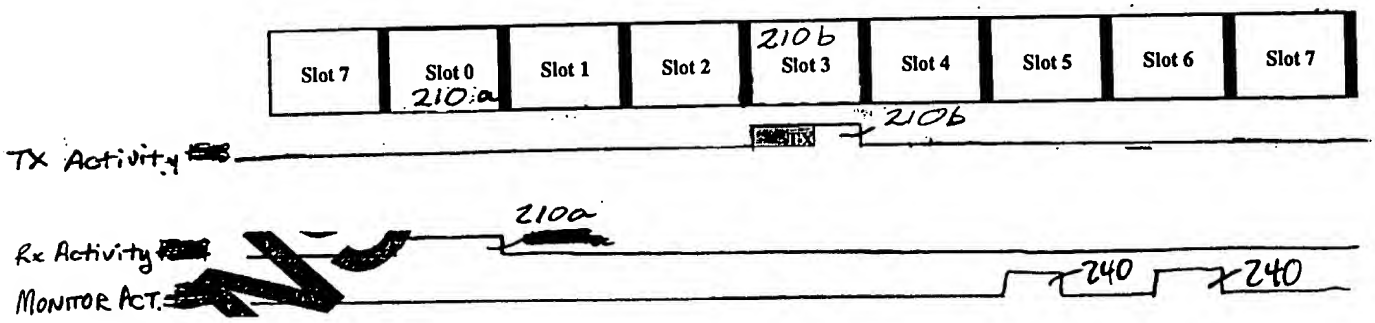


FIGURE 2B

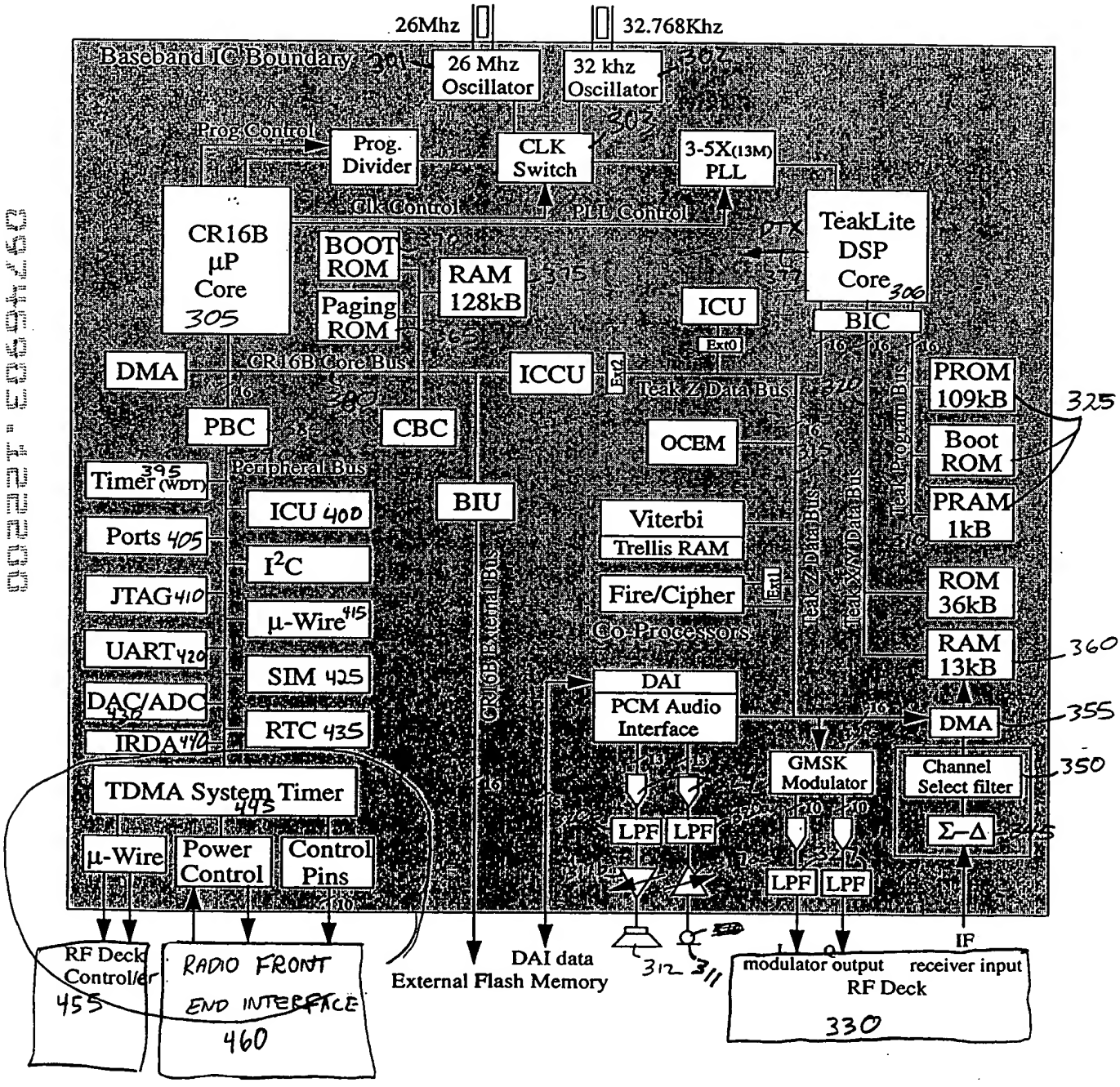

26Mhz
32.768Khz
Baseband IC Boundary 301
26 Mhz Oscillator
32 khz Oscillator
302
303
Prog. Control
Prog. Divider
CLK Switch
3-5X(13M) PLL
Clk Control
PLL Control
CR16B µP Core 305
BOOT ROM 370
Paging ROM 365
RAM 128kB 375
377
ICU
TeakLite DSP Core 300
BIC
Ext0
CR16B Core Bus
DMA
ICCU
Ext2
Teak Z Data Bus 320
PROM 109kB
325
Boot ROM
PBC
CBC
OCEM
Peripheral Bus
Timer (WDT) 395
ICU 400
BIU
PRAM 1kB
Viterbi Trellis RAM
Ports 405
I²C
JTAG 410
µ-Wire 415
Fire/Cipher
Ext1
Teak Z Data Bus
Teak XY Data Bus
Teak Program Bus
ROM 36kB
Co-Processors
UART 420
SIM 425
RAM 13kB
360
DAC/ADC 430
RTC 435
DAI
PCM Audio Interface
DMA
355
IRDA 440
CR16B External Bus
GMSK Modulator
Channel Select filter
350
TDMA System Timer 445
LPF
Σ–Δ
µ-Wire
Power Control
Control Pins
RF Deck Controller 455
RADIO FRONT END INTERFACE 460
DAI data
External Flash Memory
312
311
IF
modulator output
receiver input
RF Deck
330

FIGURE 3

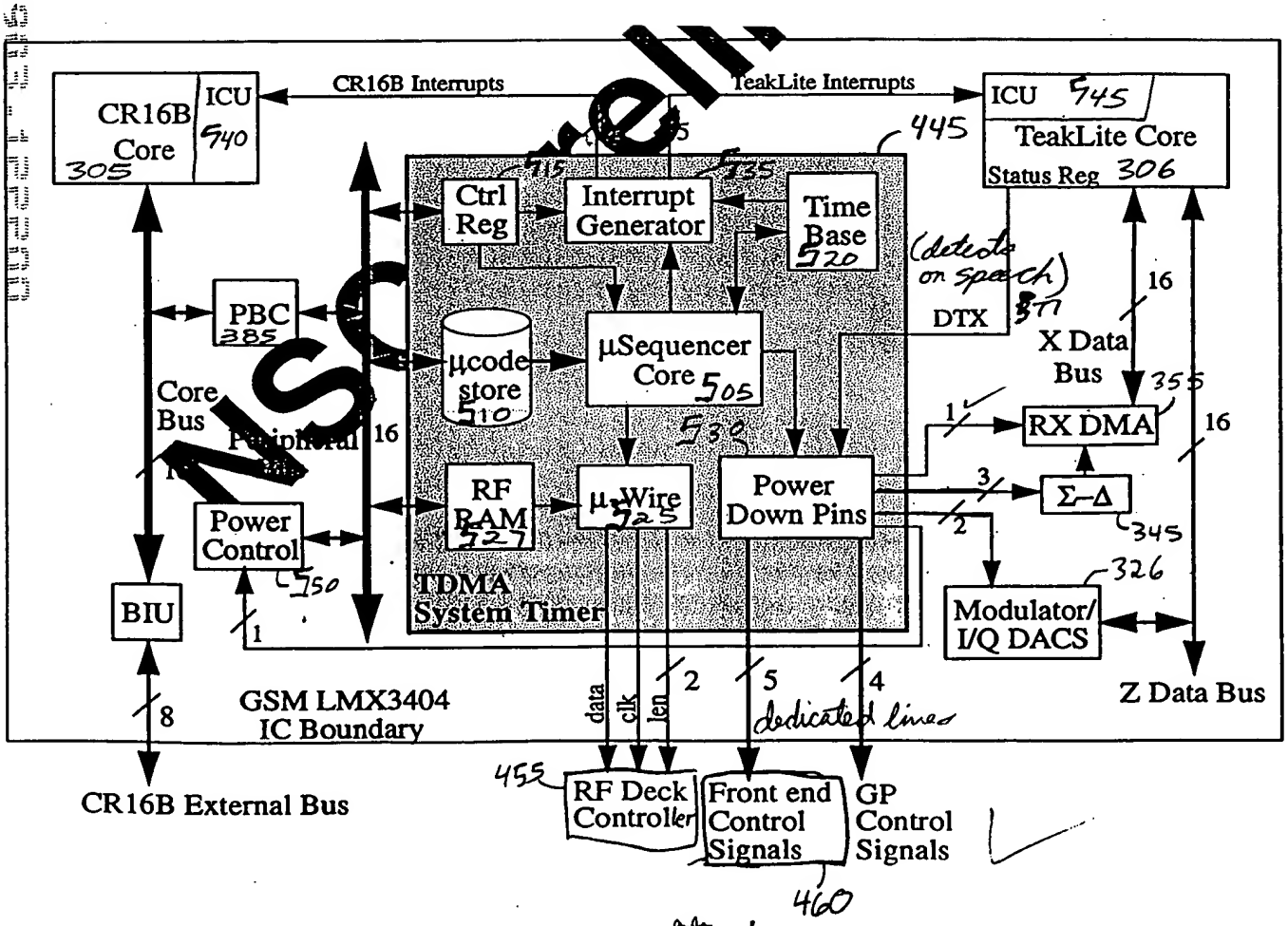
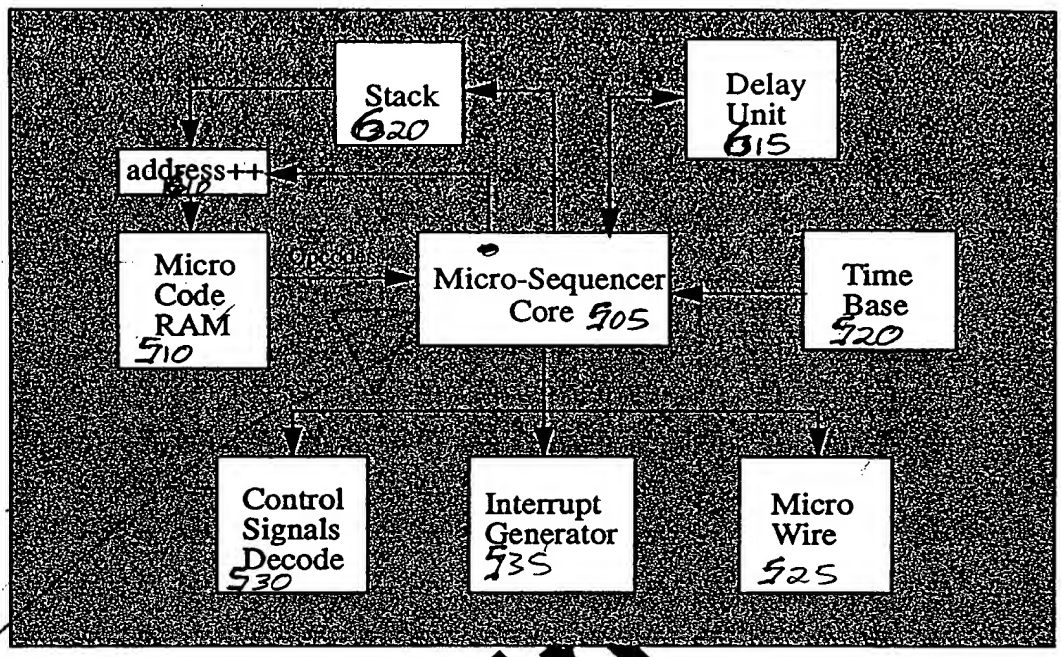

CR16B Core
ICU
CR16B Interrupts
TeakLite Interrupts
ICU
TeakLite Core
Status Reg
Ctrl Reg
Interrupt Generator
Time Base
PBC
µcode store
µSequencer Core
DTX
(detects on speech)
X Data Bus
Core Bus
Peripheral
RF RAM
µ-Wire
Power Down Pins
RX DMA
Σ-Δ
Power Control
BIU
TDMA System Timer
Modulator/ I/Q DACS
Z Data Bus
GSM LMX3404 IC Boundary
data
clk
len
dedicated lines
CR16B External Bus
RF Deck Controller
Front end Control Signals
GP Control Signals

FIGURE 4


Stack
620
Delay
Unit
615
address++
Micro
Code
RAM
510
opcode
Micro-Sequencer
Core 505
Time
Base
520
Control
Signals
Decode
530
Interrupt
Generator
535
Micro
Wire
525

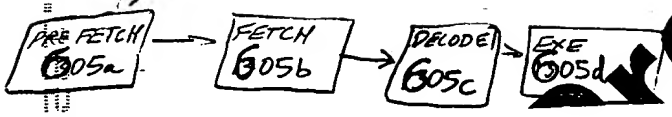

PRE FETCH
605a
FETCH
605b
DECODE
605c
EXE
605d

FIG. 5

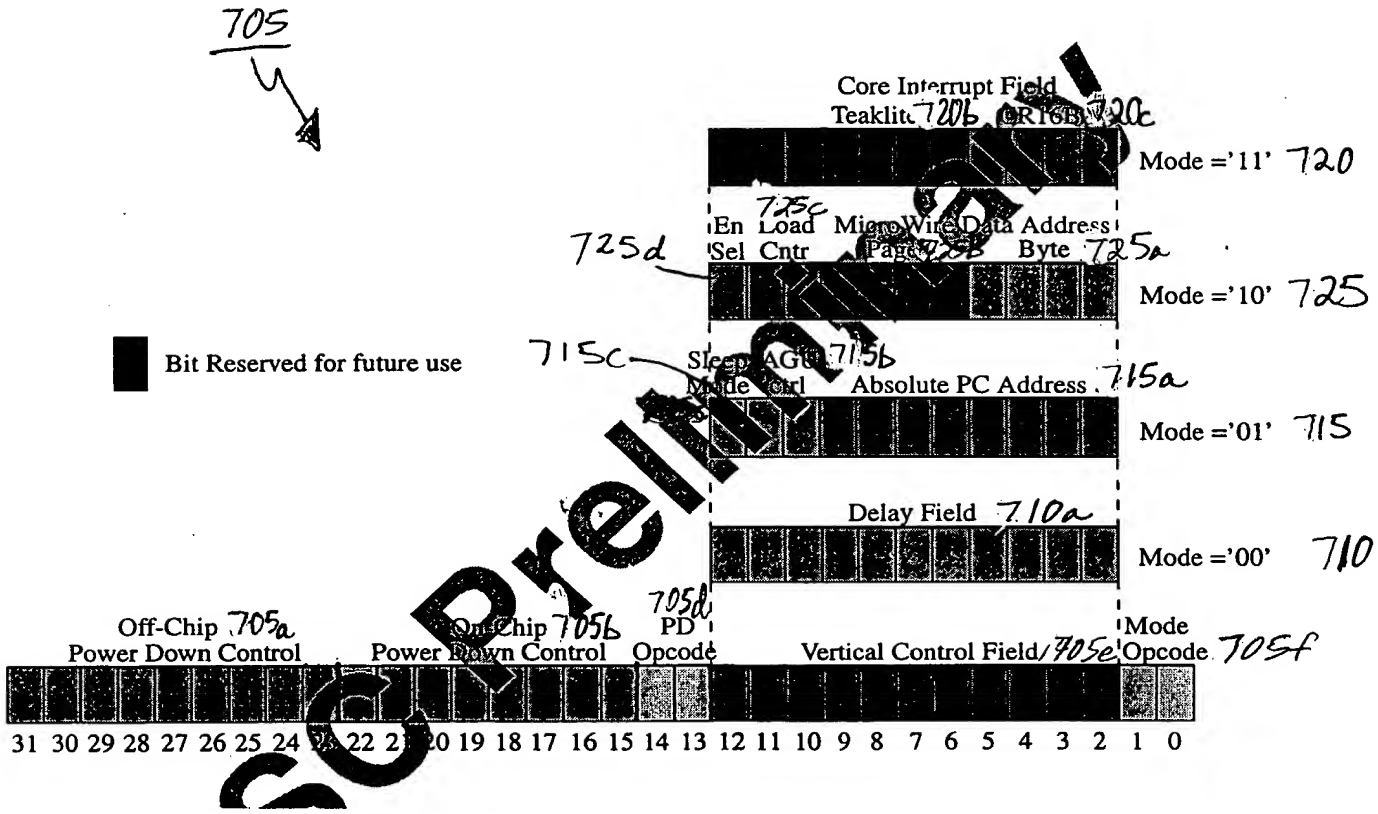


FIGURE 6

Preliminary

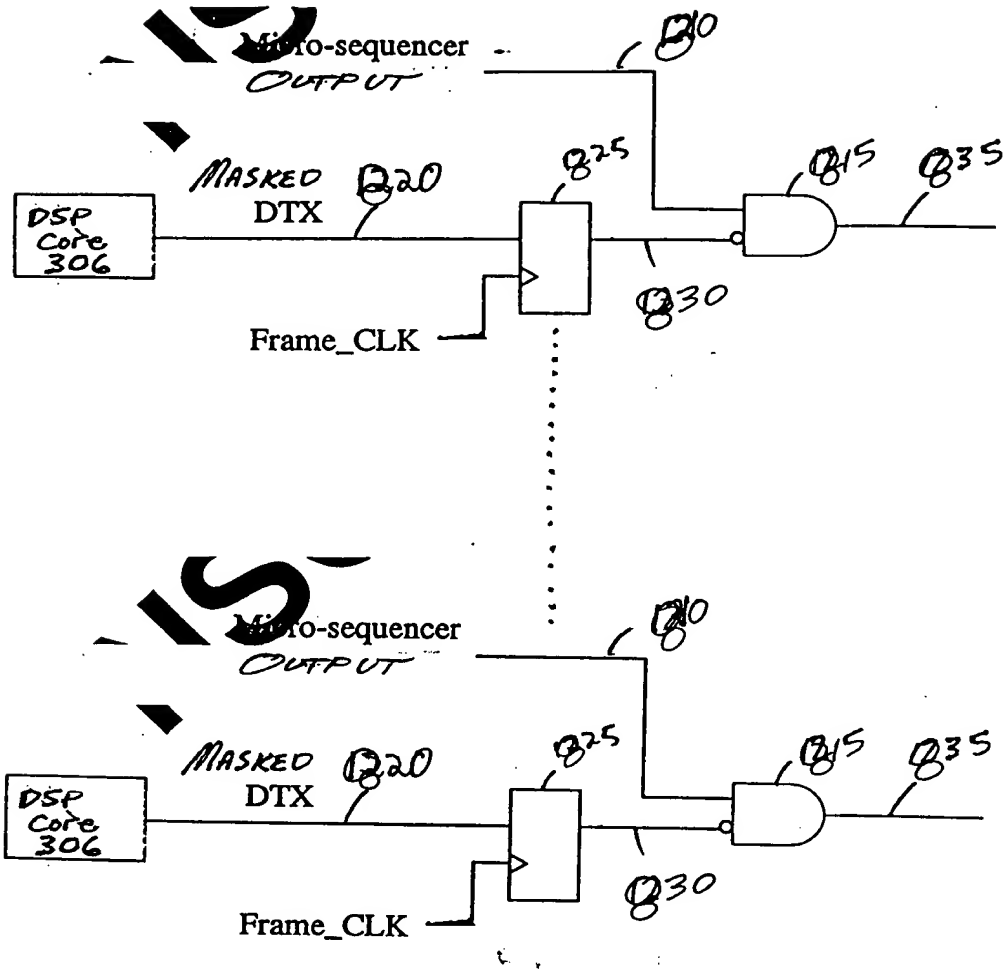

Micro-sequencer
OUTPUT
810
MASKED
DTX
820
DSP
Core
306
825
815
835
830
Frame_CLK
Micro-sequencer
OUTPUT
810
MASKED
DTX
820
DSP
Core
306
825
815
835
830
Frame_CLK

FIGURE 7

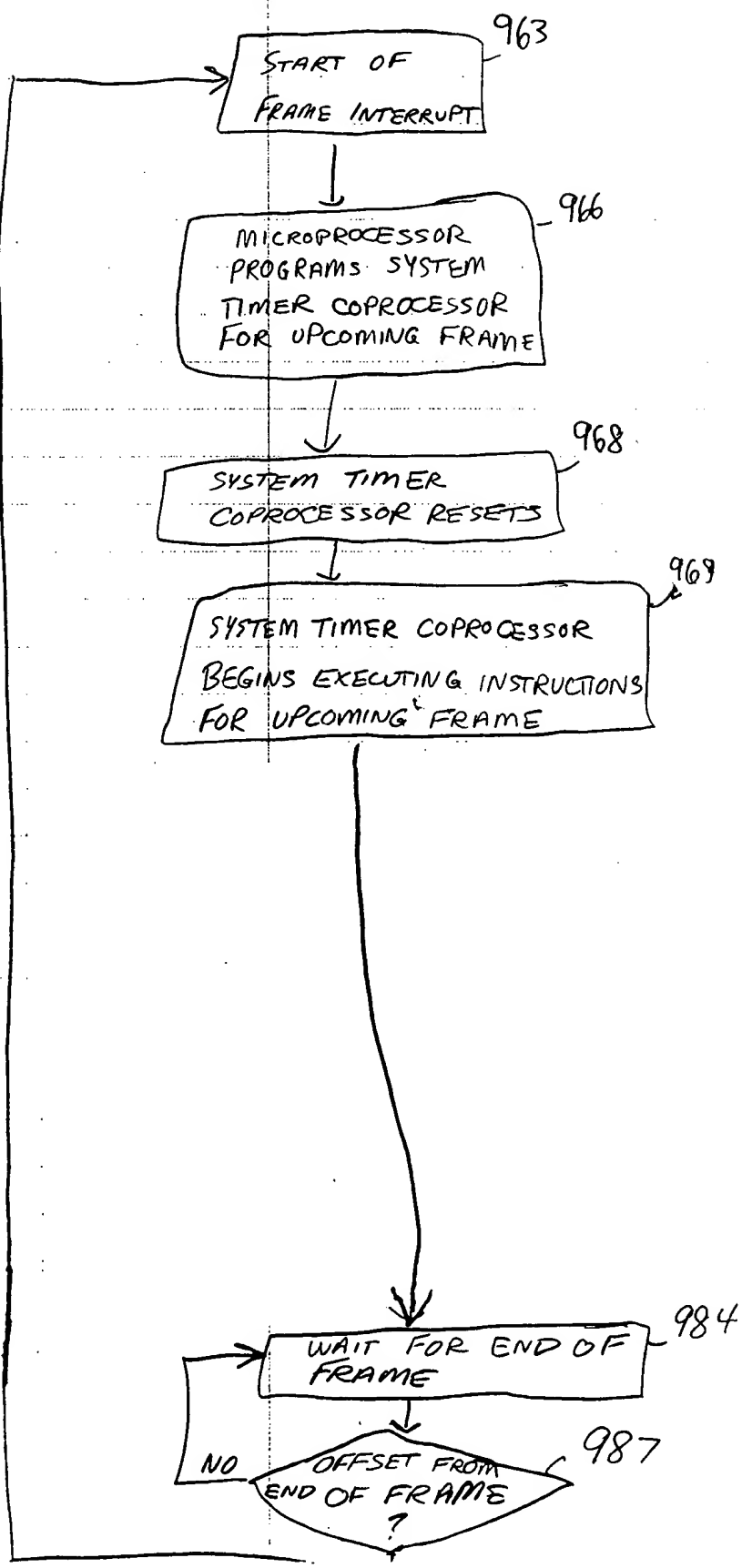
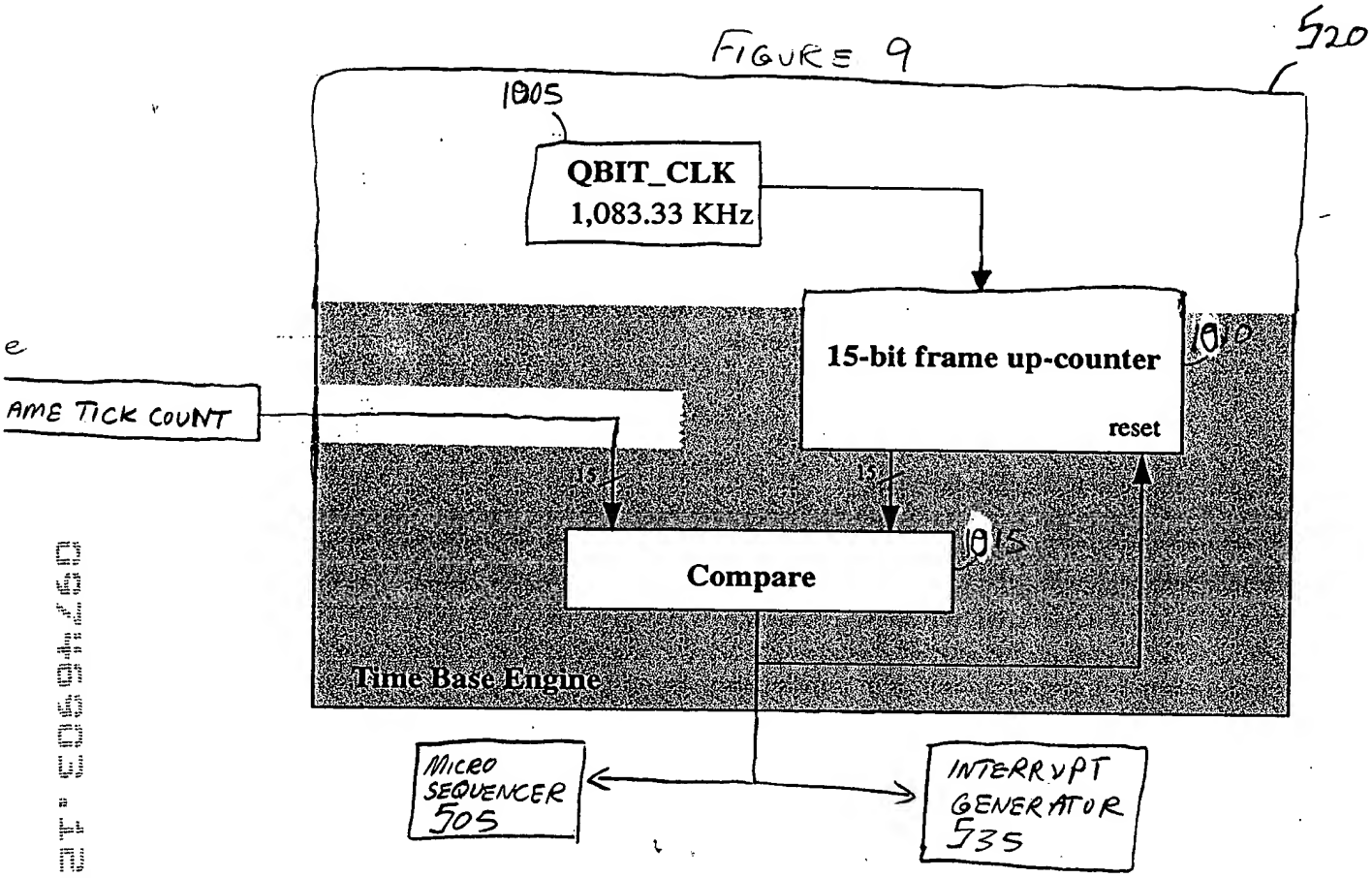

963
START OF FRAME INTERRUPT
966
MICROPROCESSOR PROGRAMS SYSTEM TIMER COPROCESSOR FOR UPCOMING FRAME
968
SYSTEM TIMER COPROCESSOR RESETS
969
SYSTEM TIMER COPROCESSOR BEGINS EXECUTING INSTRUCTIONS FOR UPCOMING FRAME
984
WAIT FOR END OF FRAME
987
NO
OFFSET FROM END OF FRAME ?

FIGURE 8

FIGURE 9



Conexant - Exhibit 2005 - Page 104

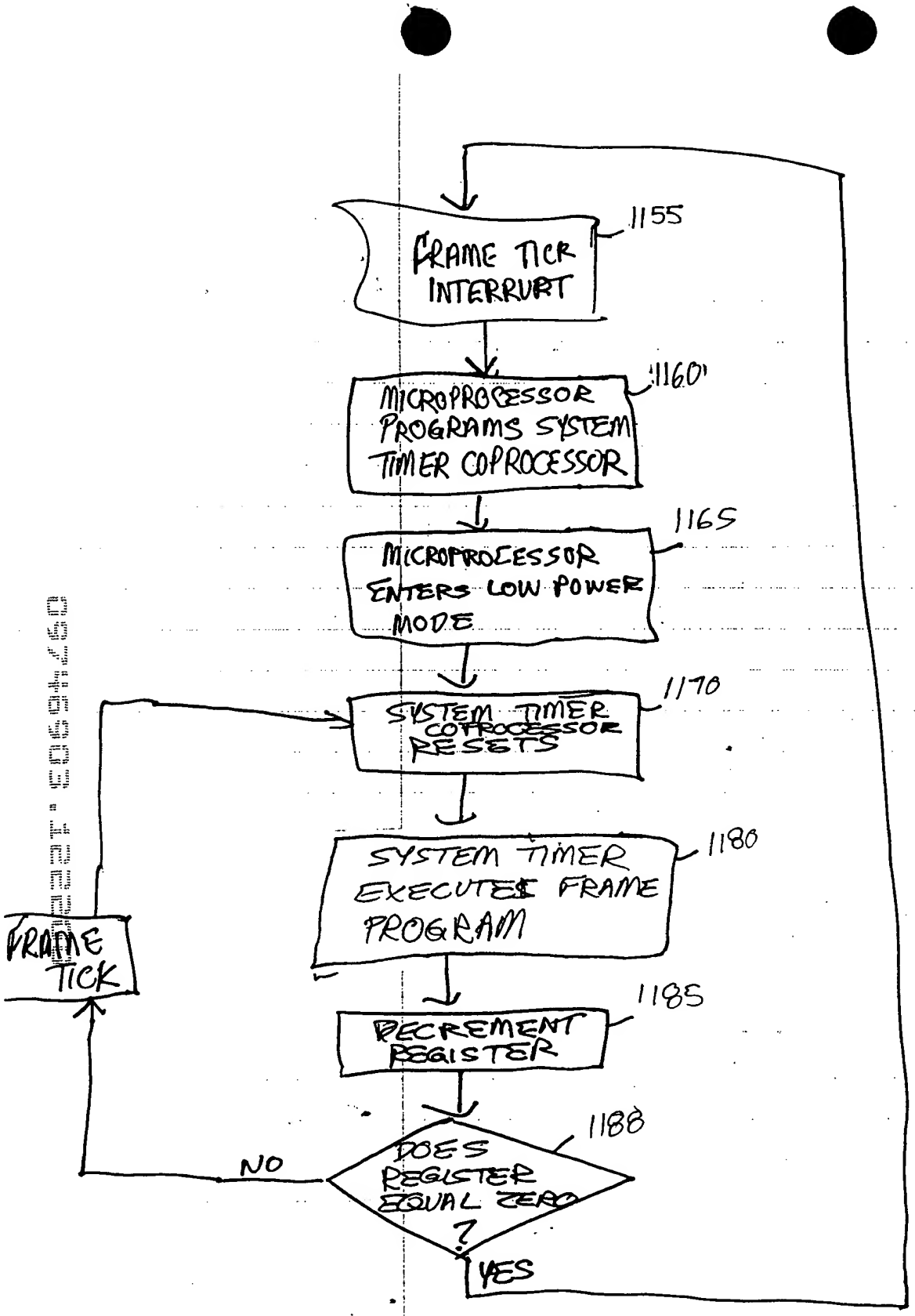

FRAME TICK INTERRUPT
1155
MICROPROCESSOR PROGRAMS SYSTEM TIMER COPROCESSOR
1160
MICROPROCESSOR ENTERS LOW POWER MODE
1165
SYSTEM TIMER COPROCESSOR RESETS
1170
SYSTEM TIMER EXECUTES FRAME PROGRAM
1180
DECREMENT REGISTER
1185
DOES REGISTER EQUAL ZERO ?
1188
NO
YES
FRAME TICK

FIGURE 10

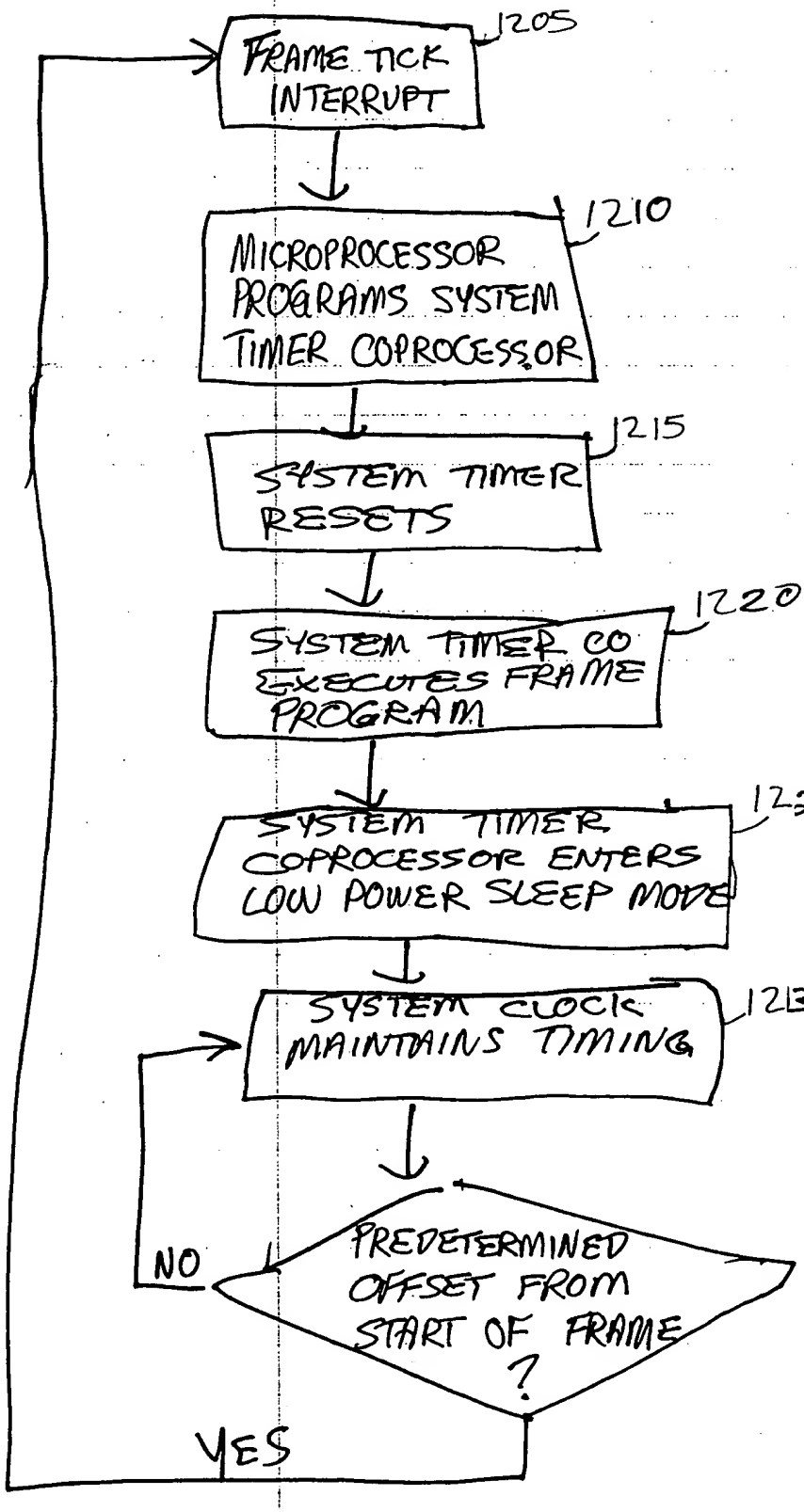

FRAME TICK INTERRUPT
1205
MICROPROCESSOR PROGRAMS SYSTEM TIMER COPROCESSOR
1210
SYSTEM TIMER RESETS
1215
SYSTEM TIMER CO EXECUTES FRAME PROGRAM
1220
SYSTEM TIMER COPROCESSOR ENTERS LOW POWER SLEEP MODE
1225
SYSTEM CLOCK MAINTAINS TIMING
1230
PREDETERMINED OFFSET FROM START OF FRAME ?
NO
YES

FIG. 11

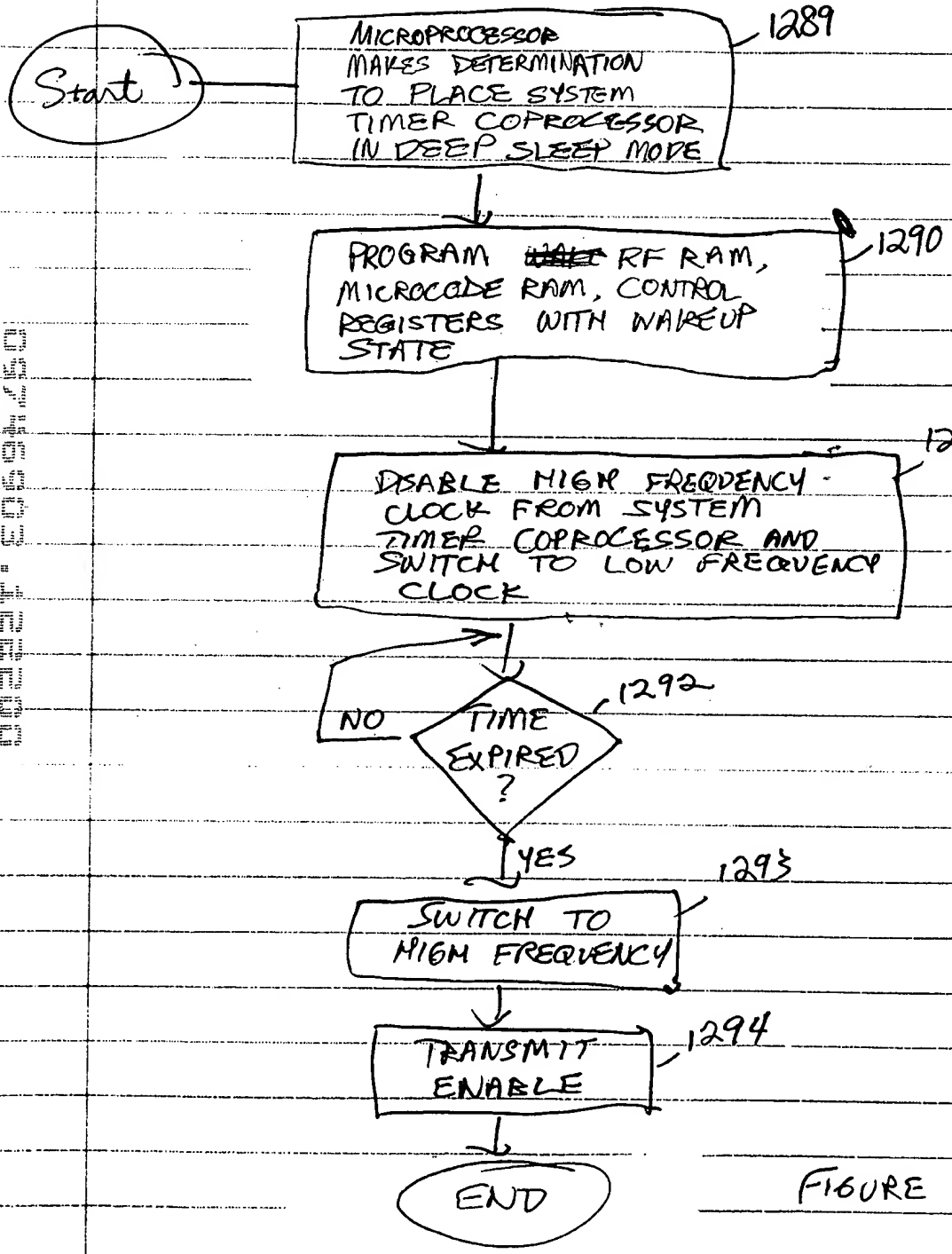

Start
MICROPROCESSOR MAKES DETERMINATION TO PLACE SYSTEM TIMER COPROCESSOR IN DEEP SLEEP MODE
1289
PROGRAM ~~WAKE~~ RF RAM, MICROCODE RAM, CONTROL REGISTERS WITH WAKEUP STATE
1290
DISABLE HIGH FREQUENCY CLOCK FROM SYSTEM TIMER COPROCESSOR AND SWITCH TO LOW FREQUENCY CLOCK
1291
NO
TIME EXPIRED ?
1292
YES
SWITCH TO HIGH FREQUENCY
1293
TRANSMIT ENABLE
1294
END

FIGURE 11B

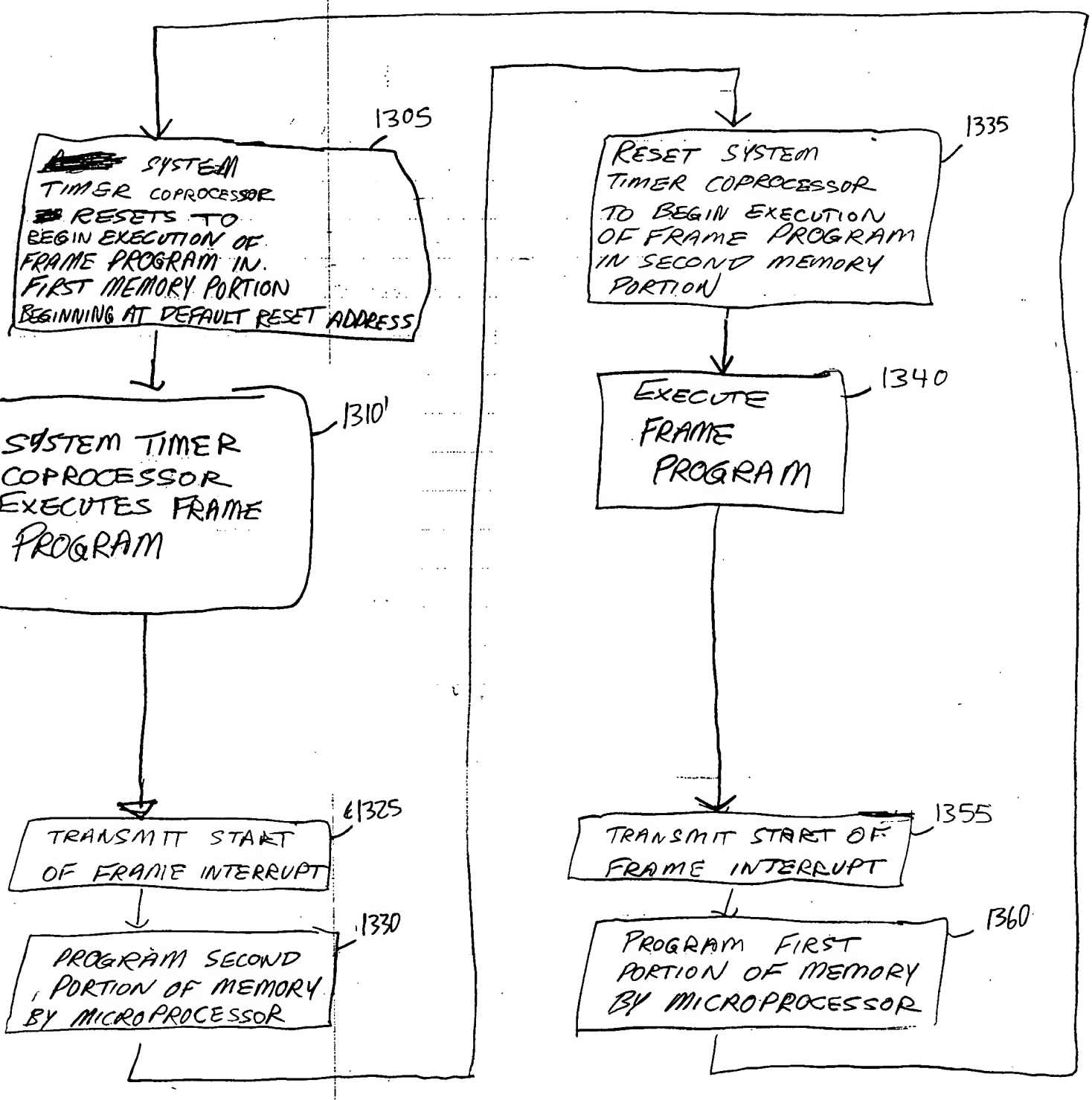

1305
SYSTEM TIMER COPROCESSOR RESETS TO BEGIN EXECUTION OF FRAME PROGRAM IN FIRST MEMORY PORTION BEGINNING AT DEFAULT RESET ADDRESS
1310'
SYSTEM TIMER COPROCESSOR EXECUTES FRAME PROGRAM
1325
TRANSMIT START OF FRAME INTERRUPT
1330
PROGRAM SECOND PORTION OF MEMORY BY MICROPROCESSOR
1335
RESET SYSTEM TIMER COPROCESSOR TO BEGIN EXECUTION OF FRAME PROGRAM IN SECOND MEMORY PORTION
1340
EXECUTE FRAME PROGRAM
1355
TRANSMIT START OF FRAME INTERRUPT
1360
PROGRAM FIRST PORTION OF MEMORY BY MICROPROCESSOR

FIGURE 12